LCL Filter Design for Grid-Connected Inverters by Analytical Estimation of PWM Ripple Voltage

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***Abstract*—LCL filter is becoming an attractive choice over conventional L filters for grid-connected voltage source inverters (VSI) due to smaller inductor size and better attenuation of the ripple components in the grid current. The modulation of the VSI generates switched voltages which results in distorted currents. In this paper, a simple closed form analytical expression is derived for the higher order switching components present in the inverter voltage. This is used in a systematic design procedure to design the LCL filter components for allowable grid current harmonics. A passive damping resistor is designed ensuring minimum power loss. The design is validated by simulations in MATLAB/Simulink and experiments on a laboratory prototype.**

Keywords*—*Voltage source inverter (VSI), Total harmonic distortion (THD), Space vector pulse-width modulation (SVPWM), Passive input filter

I. INTRODUCTION

With the advent of renewable energy generation through solar, wind, etc., grid-tied voltage source inverters (VSI) are becoming popular as the power electronic interface [1] [2]. However due to pulse width modulation (PWM) of the VSI, high frequency switched voltages are generated resulting in distortion of the grid currents. Hence an inductive L filter is generally used to couple it with the grid. However to reduce cost of copper and magnetic material of L, an LCL filter is more often used. The LCL filter results in relaxing the size of the boost inductor (inverter side) and provides better attenuation of the ripple current. In addition to grid interface for renewables, the LCL filter is also used with active front end rectifiers in industrial drives.

Design of these passive filter components requires an accurate estimation of different ripple quantities present in different voltages and currents. Along with attenuating the ripple components in the grid current, a properly designed filter must also ensure :

- high grid power factor,
- minimum voltage drop across filter,
- minimum loss in damping resistor,
- low electromagnetic interference

A proper design of the LCL filter for a VSI requires an accurate estimation of the inverter's PWM voltage ripple. In [3] [4], the PWM voltage RMS is derived using Bessel functions. In [5], the inverter voltage ripple is calculated using an approximate harmonic analysis. However above methods require complicated computations using special functions. In [6], the maximum amplitude of inverter ripple current is given through analysis of the current transient process and [7] computes the actual ripple current based on the PWM pattern. However the ripple current derived to use in filter design is itself a function of the filter component L. A simulation model is used to derive the ripple quantities in [8]. In this paper, a simple closed form analytical expression is derived for the inverter voltage ripple as a function of just the modulation index and DC-link voltage. This eliminates the need for complex calculations or estimation using a simulation model.

Different design procedures have been proposed in literature for LCL filter based on frequency domain approach [9]–[14]. Filter design using generic optimization with different constraints like ripple current in input and grid side, maximum temperature, maximum filter volume, etc. is done in [15]. To mitigate resonance effects of filter components, active and passive damping schemes have been proposed. Active damping schemes, though energy efficient require additional control complexity [16]–[21]. A simpler and more cost effective solution is to use a passive damping technique. Different filter topologies for proper passive damping have been discussed in [22]–[25].

In this paper, a systematic step-by-step design procedure is presented to calculate different filter components. The VSI is modeled for both the fundamental and switching frequency components. By the principle of superposition, both the models are independently analyzed. From these models, simultaneous design equations are derived to calculate the filter values based on allowable specifications in inverter current ripple, grid current ripple and reactive current through filter capacitor. A passive damping resistor in series with C is designed for minimum ohmic loss. The analysis of modulation and derivation of inverter voltage ripple is presented in Section II, filter design is explained in Section III, simulation and experimental results are given in Section IV and V, followed by conclusion in Section VI respectively.

II. ANALYSIS

The filter design requires modeling of the VSI for the fundamental frequency and higher frequency components. For the switching frequency component, the RMS of the inverter voltage ripple is analytically computed. Conventional space vector modulation is similar, but allows higher voltages to be synthesized, in comparison to the sine-PWM method. Therefore, it is only the conventional space vector modulation method that is considered in this paper.

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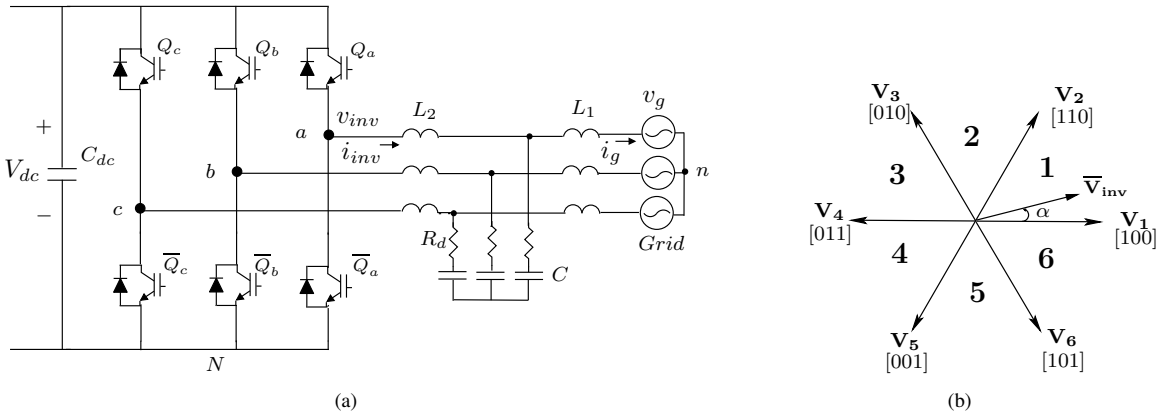


(a) (b)

Fig. 1. (a) Circuit topology of grid-connected voltage source inverter, (b) Space vectors of the VSI

A. Modulation

A voltage source inverter (VSI) generates balanced three phase voltages from a fixed DC-link, Fig. 1(a). The converter is modulated using the six active voltage space vectors as shown in Fig. 1(b). The reference voltage vector $\overline{\mathbf{V}}_{\mathbf{inv}}$ is generated from two adjacent active vectors and zero vector whose duty ratios are given by (1). Here m is the modulation index given by ratio of peak of the fundamental component of the inverter voltage V_{inv} to the DC-link voltage V_{dc} and α is the angle between the first vector and $\overline{\mathbf{V}}_{\mathbf{inv}}$. In grid tied inverters, $\overline{\mathbf{V}}_{\mathbf{inv}}$ is generated by a closed loop controller that regulates the active and reactive power flow between the DC-link and the grid. The DC-link voltage is maintained constant with a closed loop control as described in [9]. It is based on the conventional vector control scheme used in electrical machines. An outer voltage loop maintains the DC-link voltage (V_{dc}) constant and two inner current loops control the real and reactive power flow between the DC-link and the grid. The 3-line currents are converted into their corresponding $d-q$ components resulting in dc-quantities. The $d-$component of the line currents is directly proportional to the real power flow, and $q-$component determines the reactive power flow. By just transferring real power, unity power factor is maintained at the grid. Thus modulation with control results in grid power factor correction.

$$\begin{aligned} dV_1 &= \sqrt{3} m_V \sin\left(\frac{\pi}{3} - \alpha\right) \\ dV_2 &= \sqrt{3} m_V \sin\alpha \\ dV_z &= 1 - dV_1 - dV_2 \end{aligned} \tag{1}$$

B. Modeling of VSI for filter design

The modulation of the voltage source inverter generates switched voltages, v_{inv}. To the input filter the VSI appears as a voltage source for both the fundamental and switching frequency components. In this section, the modeling of the inverter for filter design is presented.

The instantaneous phase voltage referred to grid neutral (n) can be expressed in terms of three instantaneous phase voltages referred to the negative DC link (N) as given in (2). Fig. 2 shows three input phase to negative DC-link voltages and one input phase a to neutral voltage v_{an}. Considering conventional space vector pulse width modulation, over one sampling cycle in the first sector, the instantaneous input line to neutral voltage is composed of levels $2V_{dc}/3$ and $V_{dc}/3$ as shown in Fig. 2. One sampling cycle T_s is composed of time periods dV_1T_s and dV_2T_s. In the first sector, during dV_1T_s interval, when vector $\mathbf{V_1}$ [1 0 0] is applied, switches Q_a, $\overline{Q}_b$ and $\overline{Q}_c$ are ON. Hence the voltage applied across input phase a referred to DC-link negative is V_{dc} and across input phase b and c referred to DC-link negative is zero. Hence the instantaneous inverter phase a voltage referred to grid neutral is $2V_{dc}/3$ ($v_{an} = \frac{1}{3}(2V_{dc} - 0 - 0)$, Fig. 2(a). Similarly for dV_2T_s, when [1 1 0] is applied, $v_{aN} = V_{dc}$, $v_{bN} = V_{dc}$ and $v_{cN} = 0$. Thus the instantaneous input phase a voltage $v_{an} = V_{dc}/3$. Hence the RMS square of inverter line to neutral voltage over one sampling cycle in the first sector is given by (3). Similarly it is possible to obtain the expressions for the RMS square of inverter voltage over a sampling cycle in second (Fig. 2(b)) and third (Fig. 2(c)) sectors as given by (4) and (5) respectively. This computation repeats for the remaining three sectors. Now the square RMS of inverter voltage over a sector is found by (6) where ω_g is the grid frequency. Assuming the DC-link voltage to be constant, the inverter RMS voltage over one fundamental cycle is found from the RMS of each sector (7) as a function of the modulation index m (8). The ripple voltage needed for filter design is obtained by subtracting the square of fundamental component of inverter voltage from total RMS square voltage (9).

$$v_{an} = \frac{1}{3}(2v_{aN} - v_{bN} - v_{cN}) \tag{2}$$

$$v^2_{an,T_{s,1}}(rms) = dV_1\left(\frac{2V_{dc}}{3}\right)^2 + dV_2\left(\frac{V_{dc}}{3}\right)^2 \tag{3}$$

$$v^2_{an,T_{s,2}}(rms) = dV_1\left(\frac{V_{dc}}{3}\right)^2 + dV_2\left(\frac{-V_{dc}}{3}\right)^2 \tag{4}$$

$$v^2_{an,T_{s,3}}(rms) = dV_1\left(\frac{-V_{dc}}{3}\right)^2 + dV_2\left(\frac{-2V_{dc}}{3}\right)^2 \tag{5}$$

$$V^2_{an_i}(rms) = \frac{1}{\pi/3}\int_{SECTOR_i} v^2_{an,T_{s,i}}(rms)d(\omega_g t), \;\; i \equiv 1,2,3 \tag{6}$$

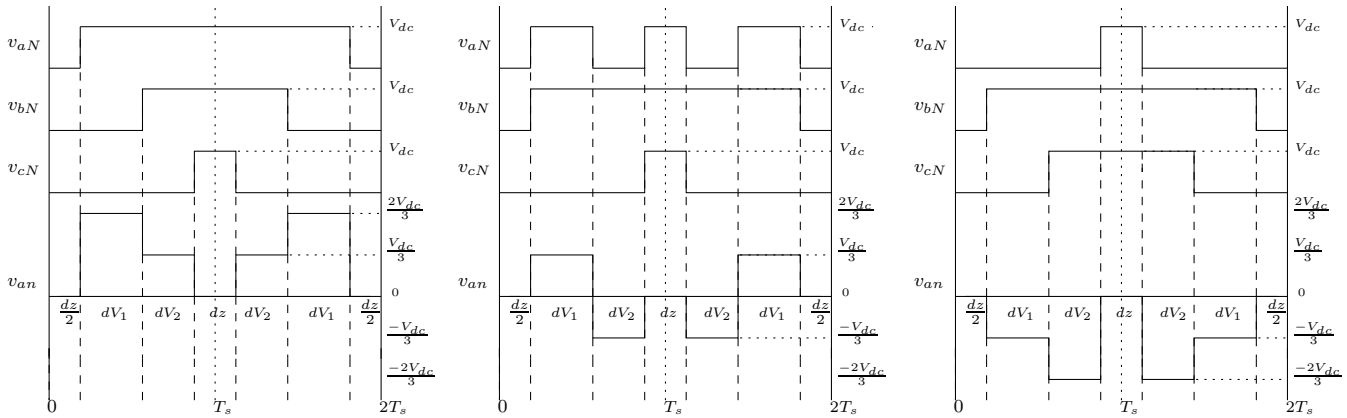


Fig. 2. Instantaneous input line to neutral voltage generation from line to negative DC-link voltages in (a) first sector, (b) second sector, (c) third sector

$$V_{an}^2(rms) = \frac{1}{3}\sum_{i=1,2,3} V_{an_i}^2(rms) \tag{7}$$

$$V_{an}^2(rms) = \frac{2\sqrt{3}}{3\pi} m V_{dc}^2 \tag{8}$$

$$V_{an_{SW}}^2(rms) = \frac{2\sqrt{3}}{3\pi} m V_{dc}^2 - V_{inv}^2(rms) \tag{9}$$

The model at switching frequency has a voltage source at frequency $1/T_s$ with the RMS given by (9). This is assuming all the ripple energy in the input voltage to be concentrated at the switching frequency f_s. The other harmonics occurring at multiples of switching frequency are all assumed to be concentrated at f_s. This results in a slight over-design of the filter components, which is a conservative approximation. For the fundamental frequency component, the VSI is modeled as a sinusoidal voltage source at line frequency (60 Hz) with RMS given by $\frac{mV_{dc}}{\sqrt{2}}$.

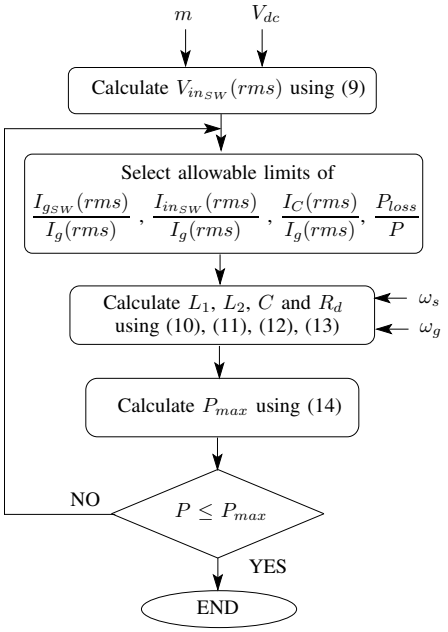


Fig. 3. Flowchart for filter design

III. FILTER DESIGN

The grid connected voltage source inverter generates switched voltages at its input which flows a distorted current. To result in smooth sinusoidal currents at the grid, an input LCL filter design is presented here. To design the filter components, the VSI is modeled for different frequency components as given in the previous section. Using principle of superposition, both these components are independently analyzed and simultaneous design equations are derived. This section presents the systematic step-by-step filter design procedure as given in the flowchart, Fig. 3.

The inverter side current ripple is restricted between 10-30% to reduce the losses due to switching currents in L_2. The grid side current THD should be within 5% according to IEEE-519 standards. The LCL filter is modeled for both fundamental (Fig. 4(a)) and switching frequency (Fig. 4(b)) components. Principle of superposition is used to consider them independently. For the ripple component, the VSI is modeled as a switching voltage source, whose RMS is given by (9). The harmonic components occur at multiples of switching frequency. As the dominant harmonics occur at the switching frequency $1/T_s$, from the filter design perspective it is assumed that all of the ripple energy is concentrated at the switching frequency ω_s. A damping resistor R_d is connected in series with the capacitor C to damp any oscillations due to resonance. The switching ripple in the inverter current of VSI and the grid current can be expressed in terms of the inverter voltage ripple as shown in (10) and (11). For the fundamental component, the inverter is modeled as a sinusoidal voltage source V_{inv}. With a larger capacitor, more reactive power flows raising the current rating of inductor L_2 and thus of the switches. But the capacitor can not be very small either which will increase the inductor size required to meet the same attenuation. Hence the capacitor current (12) is restricted to be 5-15% of grid

Fig. 4. (a) Per-phase equivalent circuit at fundamental frequency (b) Per-phase equivalent circuit at switching frequency

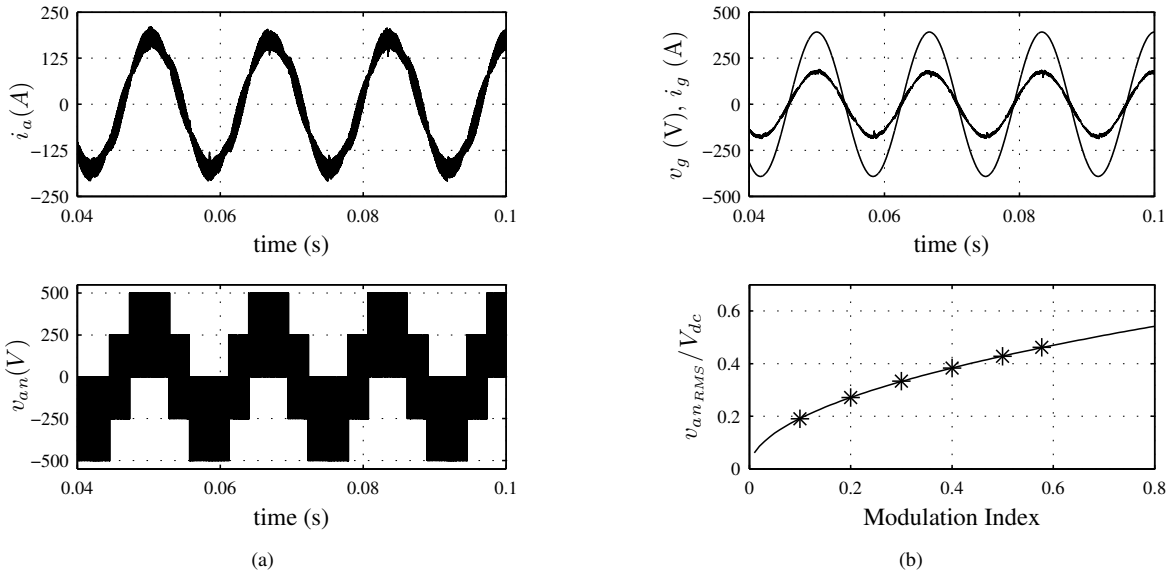


Fig. 5. Simulation Results : (a) Inverter line current and inverter line to neutral voltage (b) (top) Filtered grid current and voltage, (bottom) Variation of p.u inverter RMS voltage with modulation index

current. The power loss in the damping resistor (13) should not exceed 0.001 percent of the rated power P of the inverter. Here pf is the load power factor. The four equations can be simultaneously solved to obtain L_1, L_2, C and R_d. A design check is done with respect to the maximum power transfer possible (14). The entire design method is shown in the flowchart in Fig. 3.

$$\frac{I_{inv_{SW}}(rms)}{V_{inv_{SW}}(rms)} = \left| \frac{\left(j\omega_s L_1 - \frac{j}{\omega_s C} + R_d\right)}{j\omega_s(L_1+L_2)\left(\frac{-j}{\omega_s C} + R_d\right) - \omega_s^2 L_1 L_2} \right| \tag{10}$$

$$\frac{I_{g_{SW}}(rms)}{V_{inv_{SW}}(rms)} = \left| \frac{\left(-\frac{j}{\omega_s C} + R_d\right)}{j\omega_s(L_1+L_2)\left(\frac{-j}{\omega_s C} + R_d\right) - \omega_s^2 L_1 L_2} \right| \tag{11}$$

$$I_C(rms) = \left| \frac{V_g(rms) - j\omega_g L_1 I_g(rms)}{\frac{-j}{\omega_g C} + R_d} \right| \tag{12}$$

$$\frac{P_{loss}}{P} = \frac{3R_d I_C^2(rms)}{3V_g(rms)I_g(rms)pf} \tag{13}$$

$$P_{max} = \frac{3}{2}\frac{m_{V1}V_{dc}V_g}{\omega_g(L_1+L_2)} \tag{14}$$

IV. SIMULATION RESULTS

The analytical estimation of PWM ripple voltage and passive components design is verified by simulation in MATLAB/Simulink using ideal switches. The simulation is done implementing space vector modulation as explained in Section II. Filter design is done with the specifications of allowable THD in grid current to be 2%, total maximum ripple in inverter current to be 15%, maximum reactive current drawn by filter capacitor to be 5% and power loss in damping resistor to be 0.001% of rated values. This section presents the simulation results.

The simulation is done with ideal switches for $480V_{LL_{RMS}}$, $1MW$ VSI with modulation index $m = 0.52$ and switching frequency of $10kHz$. The DC-link voltage is controlled at $750V$ constant and reactive power flow is zero. The RMS of switching voltage ripple is calculated to be 176.74V from (9). Filter components designed for simulation are $L_1 = 37.4\mu H$, $L_2 = 160.9\mu H$, $C = 57.58\mu F$, $R_d = 1\Omega$. Fig. 5(a) shows the

inverter voltage and inverter current. The simulated inverter voltage RMS is 328.6V which almost matches the analytically computed value of 328.7V. The filtered grid current and voltage are shown in Fig. 5(b) (top). As can be seen, the grid current is nearly sinusoidal with a THD content of 1.81% and is in phase with the grid voltage showing unity power factor. The frequency spectrum of various voltages and currents is shown in Fig. 6. Fig. 5(b) (bottom) shows variation of $v_{an_{RMS}}/V_{dc}$ with modulation index. The simulated points confirm the analytically predicted continuous plots. This verifies the analytical estimation of inverter voltage RMS as described in Section II.

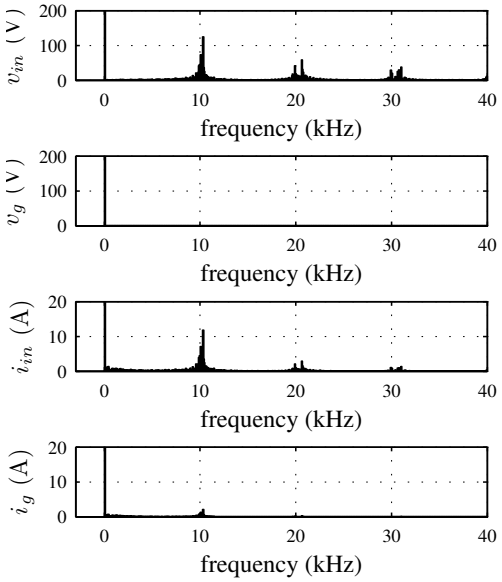


Fig. 6. Simulation Result: Frequency spectrum

V. EXPERIMENTAL RESULTS

This section presents the experimental results obtained on a scaled down laboratory prototype, Fig. 7. Integrated power IGBT module APTGF90TA60PG from Microsemi is used to implement the VSI. Integrated gate driver 6SD106EI from CONCEPT are used to generate isolated gate pulses. Control signals for space vector modulation are generated from a FPGA (Xilinx XC3S500E).

The experiments are run with a DC-link voltage of 120V and grid voltage of $55V_{LL_{RMS}}$ with a modulation index $m = 0.4$ at switching frequency of 5kHz. The designed filter components are $L_1 = 0.62mH$, $L_2 = 2.3mH$, $C = 13.94\mu F$, $R_d = 1\Omega$. Power line choke B82506-W-A6 from EPCOS ($0.5mH$, 25A) with fixed inductor 2313-V-RC ($120\mu H$, 7A) from Bourns is used in series for L_1. For L_2, fixed inductor 1140-222K-RC ($2.2\mu F$, 7A) from Bourns is used. AC film capacitors ECQU2A225KL from Panasonic of rating 2.2μF, 275 VAC are cascaded in parallel to form 4.4μF and connected in delta. This effectively makes $3 \times 4.4 = 13.2\mu$F in star connection for the filter capacitor. A 0.5W, 1Ω resistor is used as the damping resistor.

Unlike simulation where everything is ideal, dead time compensation is used between switchings in the leg. A dead time of $2\mu sec$ is used. The non-filtered inverter voltage and current are shown in Fig. 8(a). The RMS of the inverter voltage is 46.4V and the analytical value from (8) is 46.2V. Unlike simulation, the synthesized inverter voltage has voltage spikes during dead time commutation interval. The filtered waveforms and the FFT are shown in Fig. 8(b) and Fig. 9 respectively. As can be seen, the grid current is almost sinusoidal with unity power factor correction. This is verified from the FFT plot Fig. 9 which shows very low THD content in the grid current spectrum.

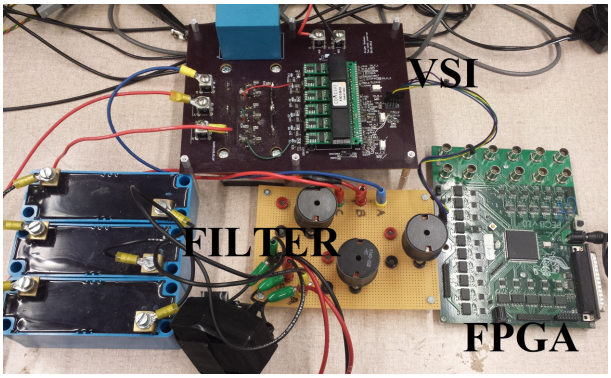


Fig. 7. Hardware setup

VI. CONCLUSION

A systematic step-by-step design procedure is presented of LCL filter design for grid connected voltage source inverters. A closed form analytical expression is derived for the inverter RMS voltage ripple based on modulation theory as a function of the modulation index and the DC-link voltage. The inverter is modeled for different frequency components and simultaneous design equations are derived to calculate the filter parameters. The design is based on specifications of allowable ripple in grid and inverter current and allowable reactive power drawn by filter capacitor. The designed filter provides sufficient THD elimination with minimum ohmic loss across damping resistor. The analytical expression and filter design are verified by simulations and experiments.

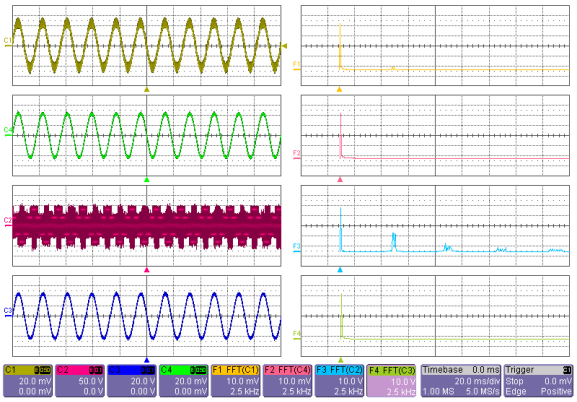
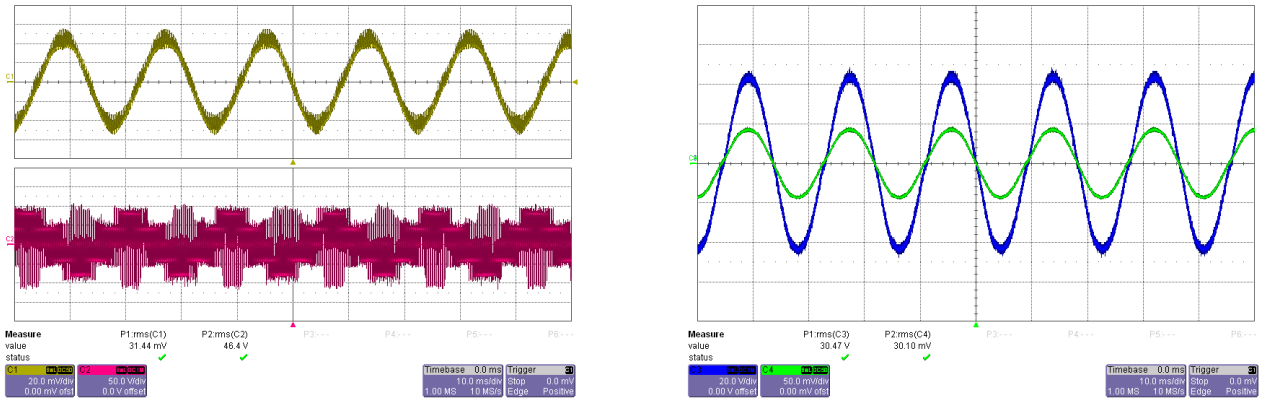


Fig. 9. Frequency spectrum : Inverter and grid currents (2A/div), inverter voltage (50V/div), grid voltage (20V/div) with corresponding FFT



(a) (b)

Fig. 8. Experimental Results : (a) Inverter line current (2A/div) and line to neutral voltage (50V/div) (b) Filtered grid current (5A/div) and voltage (20V/div)

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